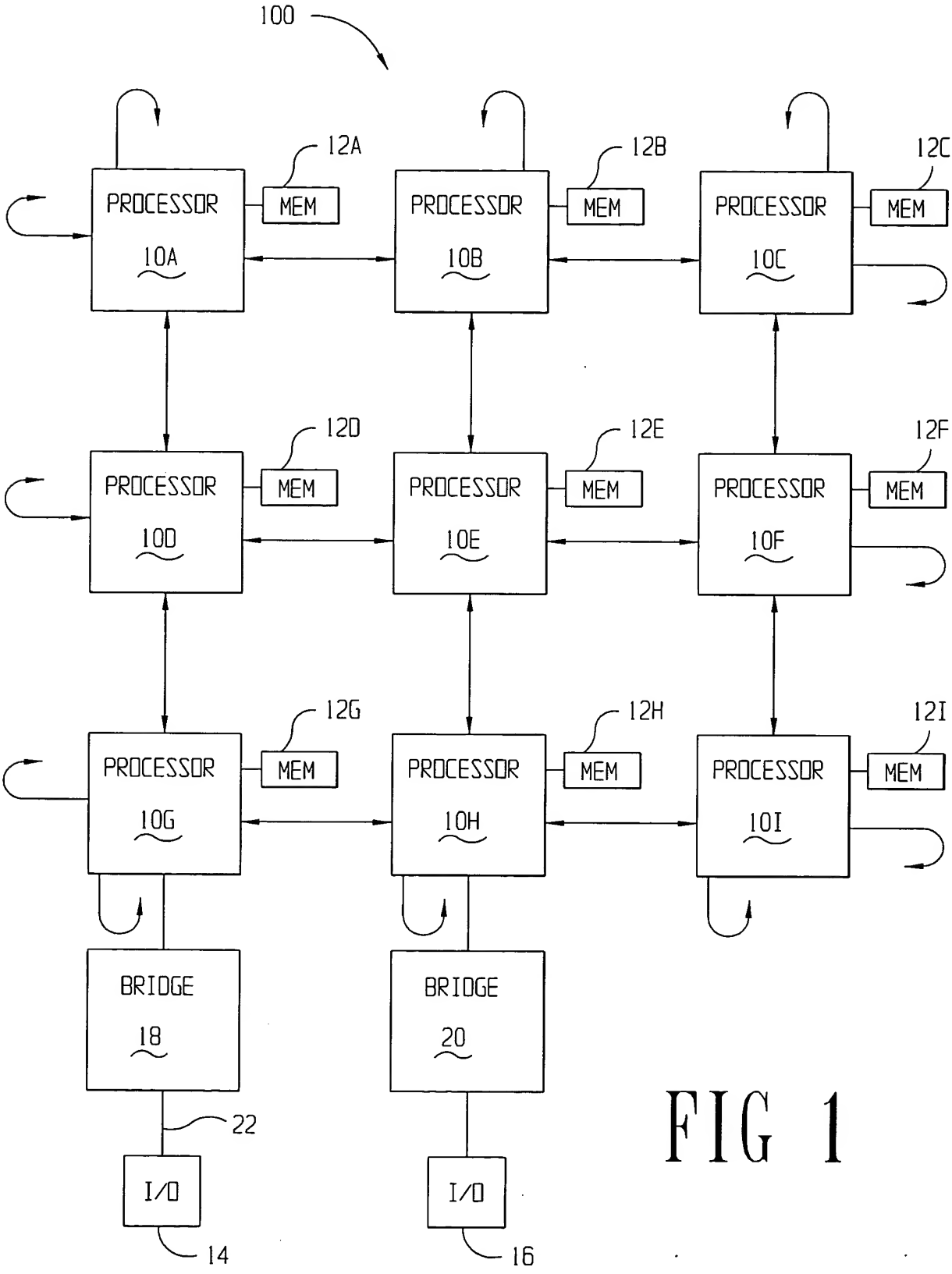
100
PROCESSOR
10A
MEM
12A
PROCESSOR
10B
MEM
12B
PROCESSOR
10C
MEM
12C
PROCESSOR
10D
MEM
12D
PROCESSOR
10E
MEM
12E
PROCESSOR
10F
MEM
12F
PROCESSOR
10G
MEM
12G
PROCESSOR
10H
MEM
12H
PROCESSOR
10I
MEM
12I
BRIDGE
18
BRIDGE
20
22
I/O
I/O
14
16

FIG 1

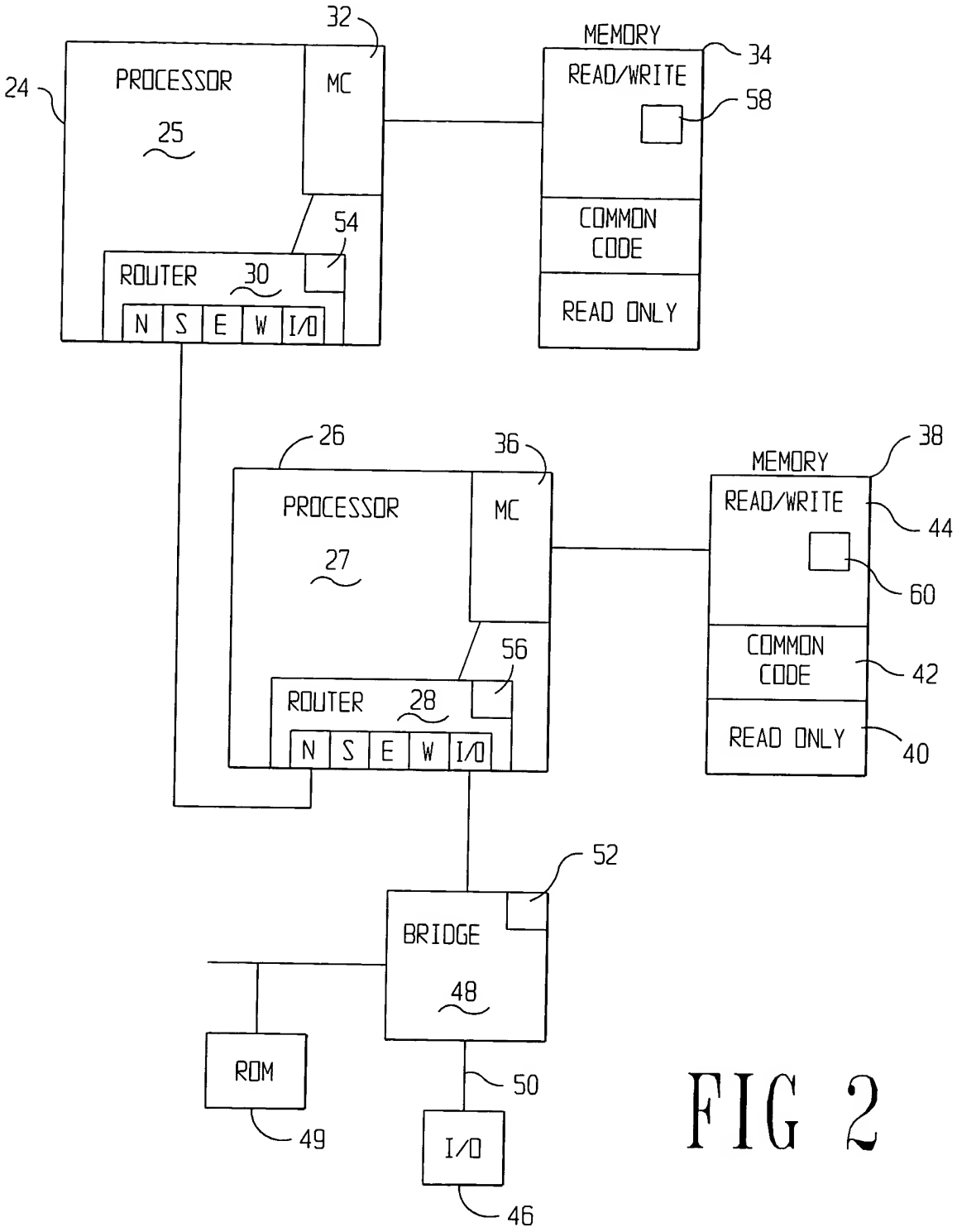
32
24
PROCESSOR
25
MC
MEMORY
34
READ/WRITE
58
COMMON CODE
READ ONLY
54
ROUTER
30
N
S
E
W
I/O
26
36
38
PROCESSOR
27
MC
MEMORY
READ/WRITE
44
60
56
COMMON CODE
42
ROUTER
28
READ ONLY
40
52
BRIDGE
48
ROM
49
50
I/O
46

FIG 2

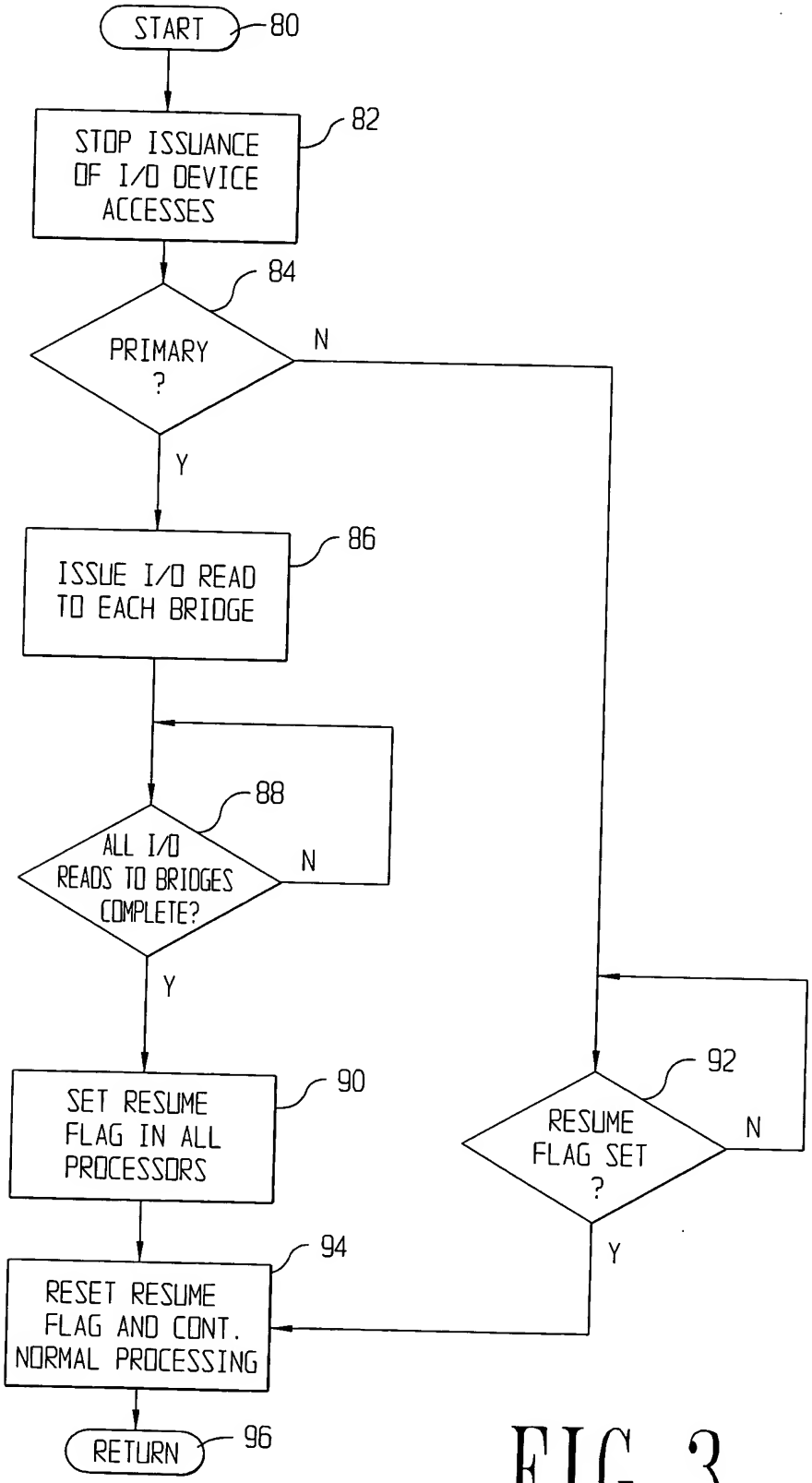
START
80
STOP ISSUANCE OF I/O DEVICE ACCESSES
82
84
PRIMARY ?
N
Y
ISSUE I/O READ TO EACH BRIDGE
86
88
ALL I/O READS TO BRIDGES COMPLETE?
N
Y
SET RESUME FLAG IN ALL PROCESSORS
90
92
RESUME FLAG SET ?
N
Y
94
RESET RESUME FLAG AND CONT. NORMAL PROCESSING
RETURN
96

FIG 3